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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,999	03/16/2004	Nobutaka Kitagawa	250561US2S	1596

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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Notice of Allowability	Application No. 10/800,999	Applicant(s) KITAGAWA, NOBUTAKA	
	Examiner Zeev Kitov	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/26/05*.

2. ☒ The allowed claim(s) is/are *3 and 5*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 09/26/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

Examiner acknowledges a submission of IDS filed on September 26, 2005. Accordingly, the Supplemental Office Action is issued.

The following is an examiner's statement of reasons for allowance:

An amended independent Claim 3 discloses, inter alia, an NMOS transistor having drain and source terminals connected between the base and the emitter of the NPN type bipolar transistor and a gate terminal supplied with a control signal of the control circuit. The closest reference for the claim is Hulfachor et al. (US 2003/0026054), which discloses some of the claim limitations, such as an NPN type bipolar transistor having a collector and an emitter connected between a first power supply terminal and a reference terminal in the semiconductor device to be protected; a control circuit outputting a control signal in response to a voltage emerging on the first power supply terminal; and a logical circuit having an output terminal connected to the gate of NESD transistor and to the base of the NPN type bipolar transistor performing a logical operation based on a voltage on a second power supply terminal in the semiconductor device to be protected and the control signal of the control circuit. It further discloses the PMOS transistor having a drain terminal and a source terminal connected between a base and the collector of the NPN bipolar transistor, and supplying a base current to the base of the NPN type bipolar transistor. However, it does not disclose an NMOS transistor having drain and source terminals connected between the base and the

emitter of the NPN type bipolar transistor and a gate terminal supplied with a control signal of the control circuit, which in combination with other limitations makes the claim allowable.

Another reference is Japanese Patent Application JP 1132089, which discloses the PMOS transistor connected between a base and the collector of the NPN bipolar transistor and supplying a base current to the NPN transistor. However, it does not disclose the NMOS transistor connected between the base and the emitter of the NPN bipolar transistor. Attempt to combine two mentioned references together would not work, because the NMOS transistor in the Hulfachor et al. reference performs the same function as PMOS transistor in the JP 1132089, i.e. switching the NPN bipolar transistor on upon detection of the ESD event, therefore such inclusion of additional transistor would be redundant, and accordingly, there is no proper motivation for combining them.

Another amended independent Claim 5, discloses, inter alia, an NOR circuit configured to receive a voltage on said power supply terminal and the control signal of said control circuit. The closest reference for the claim is Hulfachor et al., which discloses a control circuit outputting a control signal in response to an over-voltage; a logical circuit performing a logic inversion function and having an output terminal connected to a base of the NPN type bipolar transistor and performing a logical operation based on a voltage on a power supply terminal of the semiconductor device to be protected and the control signal of the control circuit and to supplying a base current from the output terminal to the base of the NPN type bipolar transistor. However, it does not disclose an NOR circuit configured to receive a voltage on said power supply

terminal and the control signal of said control circuit, which in combination with other limitations makes the claim allowable.

Japanese Patent Office in its action expressed opinion "No particular inventive effort would be required for or no particular difficulty would be found in using a NOR circuit in an arbitrary logic circuit". Examiner agrees with this statement being taken as a general concept. However, using the NOR gate to perform a logic operation based on a signal from a power supply terminal of the semiconductor device to be protected and a signal from the control signal from the control circuit was neither found in the prior art of the record, nor supported by the prior art provided by the Japanese Patent Office.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
10/14/2005

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800